MODEL NO : _____

MODEL VERSION: 00

SPEC VERSION : Ver 2.0

ISSUED DATE: 2016-04-01

■**Preliminary Specification**
□**Final Product Specification**

Customer :_____

Approved by	Notes

Prepared by	Checked by	Approved by

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Record of Revision

Rev	Issued Date	Description	Editor
1.0	2015-12-29	Preliminary Specification Release	Xunqiang Ji
2.0	2016-04-01	Modify Mechanical Drawing & Add Packing Drawing	Xunqiang Ji

1 General Specifications

Feature		Spec
Display Spec.	Size	3.4 inch
	Resolution	800(RGB) x 800
	Technology Type	a-Si
	Pixel Configuration	R.G.B. Vertical Stripe
	Pixel pitch(um)	109.5*109.5
	Display Mode	SFT
	Surface Treatment	HC
	Viewing Direction	FREE
Mechanical Characteristics	Module (W x H x D) (mm) with CTP	99.0 x 96.6 x 3.98
	Active Area(mm)	87.6*87.6
	With /Without TSP	With CTP
	Matching Connection Type	FPC
	LED Numbers	8 LEDs
	CTP Surface hardness	≥7H
	Weight (g)	TBD
Electrical Characteristics	Interface	MIPI 3 lane
	Color Depth	16.7M
	LCD Driver IC	ILI9881C
	CTP Driver IC	HX8526-E30
	CTP Interface	IIC

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: Q/S0002

Note 3: LCM weight tolerance: ± 5%

2 Input/Output Terminals

2.1 LCD Interface

Pin No.	Symbol	I/O	Function	Remark
1	GND	GND	Power Ground	
2	LEDA	P	LED Anode	
3	LEDA	P		
4	LEDK	P	LED Cathode	
5	LEDK	P		
6	GND	GND	Power Ground	
7	VDD(-5V)	P	-5V INPUT	
8	VDD(-5V)	P		
9	GND	GND	Power Ground	
10	VDD(+5V)	P	+5V INPUT	
11	VDD(+5V)	P		
12	GND	GND	Power Ground	
13	IOVCC	P	Power supply 1.8V	
14	IOVCC	P		
15	GND	GND	Power Ground	
16	RESET	I	Global Reset Pin	
17	GND	GND	Power Ground	
18	TE	I	tearing effect output	
19	GND	GND	Power Ground	
20	NC	N	No connect	
21	NC	N		
22	NC	N		
23	GND	GND	Power Ground	
24	LAN2_P	I	MIPI lane 2+	
25	NC	N	No connect	
26	LAN2_N	I	MIPI lane 2-	
27	GND	GND	Power Ground	
28	CLK_P	I	MIPI clock +	
29	NC	N	No connect	

30	CLK_N	I	IMIPI clock -	
31	GND	GND	Power Ground	
32	LAN1_P	I	MIPI lane 1+	
33	NC	N	No connect	
34	LAN1_N	I	MIPI lane 1-	
35	GND	GND	Power Ground	
36	LAN0_P	I	MIPI lane 0+	
37	NC	N	No connect	
38	LAN0_N	I	MIPI lane 0-	
39	GND	GND	Power Ground	

2.2 CTP Interface

Pin	Name
1	VCCA(2.8V)
2	VCCD(1.8V)
3	SCL
4	SDA
5	GND
6	GND
7	TSIX
8	NC
9	NC
10	XRES

3 Absolute Maximum Ratings

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Power Supply Voltage	IOVCC	-0.3	3.3	V	Note1
Power Supply Voltage	VDD(+5V)	-0.3	6.5		
Power Supply Voltage	VDD(-5V)	-6.5	0.3		
Logic Supply Voltage	VCCIO	-0.3	3.3	V	
Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	80	℃	
Relative Humidity Note2	RH	--	≤95	%	Ta≤40℃
		--	≤85	%	40℃＜Ta≤50℃
		--	≤55	%	50℃＜Ta≤60℃
		--	≤36	%	60℃＜Ta≤70℃
		--	≤24	%	70℃＜Ta≤80℃
Absolute Humidity	AH	--	≤70	g/m³	Ta＞70℃

Table 3 Absolute Maximum Ratings

Note1: Input voltage include R0~R5, G0~G5, B0~B5, Dotclk, Hsync, Vsync, Enable, R/L, U/D.

4 Electrical Characteristics

4.1 LCD characteristics

GND=0V,Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		IOVCC	1.75	1.8	3.3	V	
Power Supply Voltage		VDD(+5V)	4.5	5.0	6	V	
Power Supply Voltage		VDD(-5V)	-6	-5.0	-4.5		
Input Signal Voltage	High Level	VIH	0.7*IOVCC	-	IOVCC	V	
	Low Level	VIL	0	-	0.3*IOVCC	V	

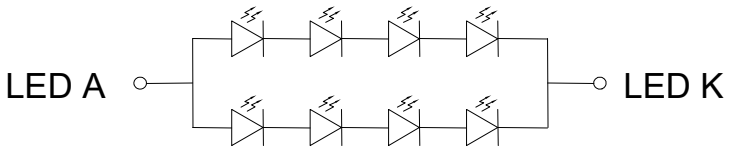
Table 4.1 LCD module electrical characteristics

4.2 Backlight Unit

Ta=25℃

Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	I_F	18	20	22	mA	1 LED
Forward Voltage	V_F	-	12.8	-	V	BLH-BLL
Backlight Power Consumption	W_{BL}	-	512	-	mW	8 LEDs
Operating Life Time	-	-	30,000	-	Hrs	For each LED

Note1: Figure below shows the connection of backlight LED.



LED CIRCUIT

(If=40mA / Vf=12.8V TYP)

Note 2: 1LED: V_F =3.2V I_F =20mA

Note 3: I_F is defined for one LED.

Optical performance should be evaluated at Ta=25℃ only.

If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

5 Timing Chart

5.1 MIPI Data to clock Timing Definition

5.1.1 High Speed Mode

High Speed Mode – Clock Channel Timing

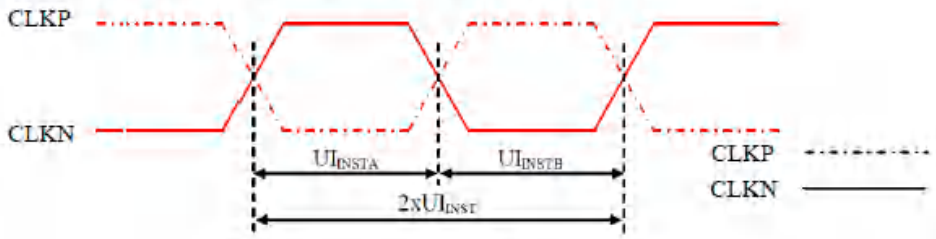


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

High Speed Mode – Data Clock Channel Timing

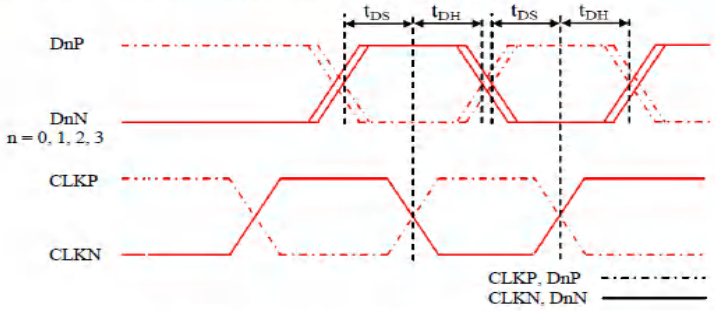


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

High Speed Mode – Rising and Falling Timings

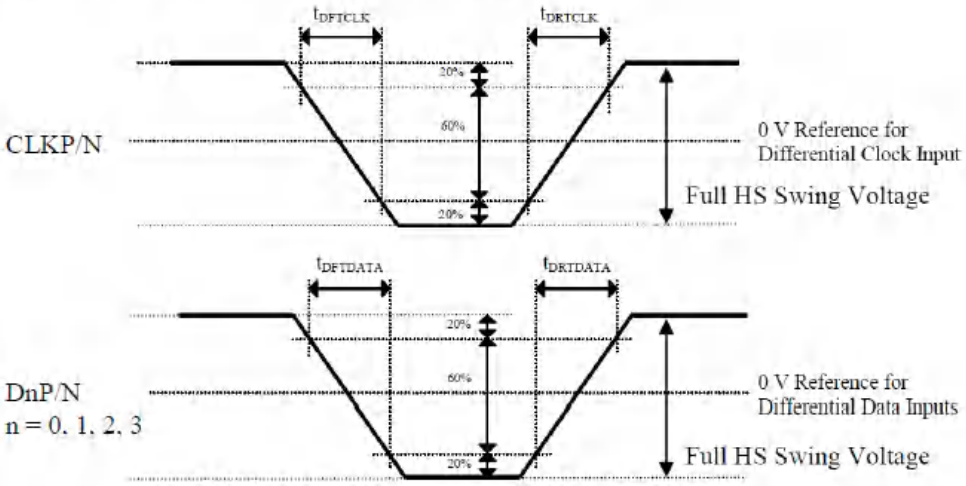


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*